

# FPGA/ASIC/DSP Portability

1. **Choose language(s): VHDL? Both Verilog? No reqt? C for DCP**
  - Language with porting likelihood; including FPGA/ASIC?
  - Coding guidelines
2. **Define IDL subset suitable for these environments**
  - IDL does NOT imply CORBA
  - Reduce data types, exceptions, etc, etc.
3. **Define mapping from that subset to a language-specific “stub/skeleton” “port” interface.**
  - Interface specifics, generated to avoid overly generic interfaces
  - Common way to understand messages, headers, fields, length etc.
4. **Define mapping to “control” interface (aka “resource/config”).**
  - Typical control (start/stop/configure), from SCA “resource”
5. **Define send/receive generic services**
  - Non-generated I/O support interfaces? (like ORB svcs?)
6. **Define environment (OE) services**
  - Clock issues, local memory issues, etc.
7. **Define deployment parameters for appropriate resources**
8. **SCA supplement “Portability Supplement for Specialized Hardware”:**
  - that contains these things analogous to the sections that tell GPP/SW authors how to write their components